REMARKS

Thorough examination and careful review of the application by the Examiner is noted and appreciated.

Claims 1-20 are pending in the application. Claims 1-20 stand rejected.

Claim Rejections Under 35 USC §103

Claims 1-10 are rejected under 35 USC §103(a) as being unpatentable over Applicant's admitted prior art (AAPA) in view of Shiromizu JP '192 and Polinsky '059.

The Examiner contended that AAPA teaches substantially the invention except the heating of the substrate to a temperature greater than 300°C in the same chamber, while such is taught by Shiromizu in heating a substrate to a temperature higher than 400°C. It is further contended that while AAPA and Shiromizu failed to teach heating the substrate for a time period greater than 30 sec., as recited in the present invention claims 3 and 4, such is taught by Polinsky in heating a substrate before a layer is formed on the substrate surface to prevent cracking.

The rejection of claims 1-10 under 35 USC §103(a) based on AAPA, Shiromizu and Polinsky is respectfully traversed.

The Applicants respectfully agree with the Examiner that AAPA does not disclose the heating of a substrate at all, while Shiromizu discloses a process of heating a substrate **to a temperature higher than 400°C, while Polinsky does not teach or disclose a temperature range at all.** In the newly amended independent claim 1, the heating step of the semiconductor substrate in the plasma CVD chamber is narrowly limited to "a temperature between 300°C and 400°C", which is clearly not taught or disclosed by AAPA, Shiromizu, Polinsky, either singularly or in combination thereof.

Moreover, the Applicants respectfully submit that Shiromizu teaches a gate oxide formation process in a furnace (by reciting "... before a gate oxide film is formed on the surface of semiconductor substrate by a heat treatment"), while AAPA and the present invention teaches the formation of an inter-metal dielectric layer by a plasma CVD process. There can be no motivation to combine the Shiromizu reference into AAPA to arrive

at the present invention process since Shiromizu and AAPA each involves a completely different technological endeavors.

In the final Office Action dated 07/08/2003, the Examiner argued in the Response To Arguments section that "the motivation for heating the substrate at 401°C before the formation of the oxide layer on the surface of the substrate in the method of AAPA is to remove the undesired organic substance on the surface of the substrate". The Applicants respectfully traverse such argument since Shiromizu discloses heating the substrate to higher than 400°C for removing organic substances, while the present invention teaches a method of heating the substrate at less than 400°C, which produces greatly improved and unexpected results such as not damaging the devices already formed on the substrate. Moreover, not only Shiromizu does not teach the present invention low temperature range, i.e. 300°C ~ 400°C, Shiromizu teaches away from the present invention novel method by disclosing a heating method at a temperature of higher than 400°C.

Moreover, the Examiner further argued that "Polinsky teaches 'the surface of a semiconductor substrate is heated before a layer is formed on the substrate surface to prevent cracking, it

would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the heating time of the substrate that allows preventing of the cracking". The Applicants respectfully traverse the arguments. First, Polinsky's heating method is aimed at solving a completely different problem than that of the present invention, i.e. Polinsky heats his substrate to prevent cracking, while the present invention teaches a heating method to outgas a substrate surface. For instance, the present invention claim 1 recites:

> "heating said semiconductor substrate in said chamber to a temperature between 300°C and 400°C for a length of time sufficient to outgas a surface of said semiconductor substrate".

The present invention therefore further claims a heating method for a length of time sufficient to degas a substrate surface, which is clearly not taught or disclosed by either Shiromizu or Polinsky. The Examiner's argument that "it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the heating time of the

substrate that allows prevention of the cracking", cannot be understood since the present invention method is not concerned with a surface cracking problem at all. As such, there can be no motivation to combine Polinsky with Shiromizu to arrive at the present invention claims.

The rejection of claims 1-10 under 35 USC §103(a) based on AAPA, Shiromizu and Polinsky is respectfully traversed. A reconsideration for allowance of these claims is respectfully requested of the Examiner.

The Applicants further submit that dependent claims 3 and 4 are separately allowable since they recite a heat treatment time limitation of "for a time period of at least 30 sec." (Claim 3), and "for a time period of at least 1 min." (Claim 4). Such time periods are clearly not taught or disclosed by either one of the three references.

Claims 11-20 are rejected under 35 USC §103(a) as being unpatentable over AAPA in view of Shiromizu JP '102 and Polinsky '059. It is contended that while AAPA and Shiromizu failed to teach heating the substrate to a period greater than 30 sec., such

is taught by Polinsky in heating a semiconductor substrate before a layer is formed on the substrate surface to prevent cracking.

The rejection of claims 11-20 under 35 USC §103(a) based on AAPA, Shiromizu and Polinsky is respectfully traversed.

Independent claim 11 was amended to more narrowly recite the invention contained therein. Claim 11, in its newly amended form, recites:

> "heat-treating said semiconductor wafer at a temperature between 300°C and 400°C for a length of time sufficient to outgas said wafer."

The Applicants respectfully submit that since AAPA fails to teach a heating process for the substrate at all, Shiromizu teaches heating the substrate to a temperature higher than 400°C, and Polinsky does not teach a range of temperature to be used for heat treating a semiconductor substrate to prevent cracking. Independent claim 11 is clearly patentable under 35 USC §103(a) based on AAPA, Shiromizu and Polinsky. A reconsideration for

allowance of claim 11, and its dependent claims 12-20, is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 1-20, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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